Keysight Technologies
W3630A Series DDR3 BGA Probes
for Logic Analyzers and Oscilloscopes

Data Sheet

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Introduction

The W3630A series DDR3 BGA probes enable probing of embedded memory DIMMs directly at the ball grid array with Keysight Technologies, Inc. logic analyzers and oscilloscopes.

The Keysight W3630A series DDR3 BGA probes for logic analyzers and oscilloscopes enable viewing of data traffic on industry standard DDR3 DRAMs with the Keysight 16900 Series and U4154A logic analysis systems and Infiniium 9000 and 90000 Series oscilloscopes.

The DDR3 BGA Probe Advantage

Features	Benefits
Connects directly to the DDR3 BGA balls.	Eliminates reflections from mid-bus probing methods. Also eliminates board space and trace routing required for connector probing methods.
Supports:	Get complete signal access to the DDR3 signals critical to your debug and validation effort.
– Single die x4, x8 and x16 configuration	
– Stacked/dual-die x4, x8 and x16 configuration	
– Stacked/quad-die x4, x8 and x16 configuration	
– Operating transfer rate of 1333 Mb/s	Operate at full speed making measurements with a Keysight U4154A logic analyzer.
– Using U4154A with APS (Advanced Probe Settings*) enabled, transfer rates up to 2400 Mb/s	
– Using 16962A with APS enabled, transfer rates up to 1600Mb/s	
– 4 GHz bandwidth (typical)	
Works with existing designs.	Eliminates need for re-design or up front planning.
Supports either leaded or lead-free solder.	Easily works with all solder finishes. Designed to tolerate lead-free soldering temperature profiles.
Contract manufactures available for those without the in-house expertise or facilities for soldering BGAs.	Eliminates the need to develop BGA soldering expertise.
Flexible "wings" with ZIF connectors.	Ensures reliable connection to the ZIF probes. Enables placement of the probe cables around adjacent components. Minimizes the torque to the balls of the BGA.
Attach to E5845A and E5847A single-ended ZIF probes for connection to the logic analyzer.	Optimizes the use of logic analyzer channels by allowing assignment of channels to 4, 8 or 16 bits on each DRAM.
Probe points available for soldering ZIF tip accessories to the scope probe adapter board that connects to the BGA probe.	Enables oscilloscope probing of the DRAM signals with a Keysight Infiniium 90000-Series oscilloscope, giving you a DDR3 test solution covering the clock characterization, electrical and timing parameters of the JEDEC specification.

* To enable Advanced Probe Settings refer to Tech brief # 5991-0799EN. Maximum transfer rates are subject to variables in the signal integrity of the system under test.

DDR3 BGA Probe Connection to a Keysight Logic analyzer

The W3631A and W3636A DDR3x16 BGA probes connect to the E5845A to provide connection to the logic analyzer. The W3633A DDR3 x4/ x8 BGA probe connects to E5847A to provide connection to the logic analyzer.

Figure 1. E5847A 46-ch single-ended ZIF probe for x8 DRAM BGA probe connects to 90-pin logic analyzer cables
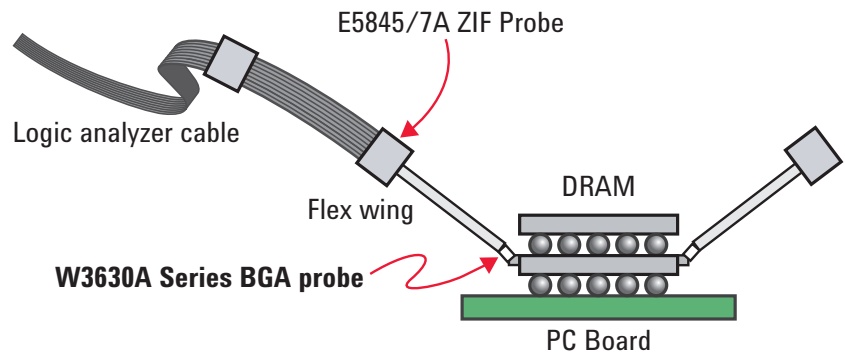
Figure 2. Probe connection to the logic analyzer

DDR EyeFinder and EyeScan Software

The DDR EyeFinder and EyeScan software is a great tool to help you position the sampling points for accurate read and write data capture. The software triggers on valid read and write commands with your system executing any memory test suite or stimulus program. The software will then display read and write data valid window as a result of the scan.

Figure 3. DDR3 EyeFinder and Eyescan software shows read and write data valid windows for accurate sampling position of data for protocol decode

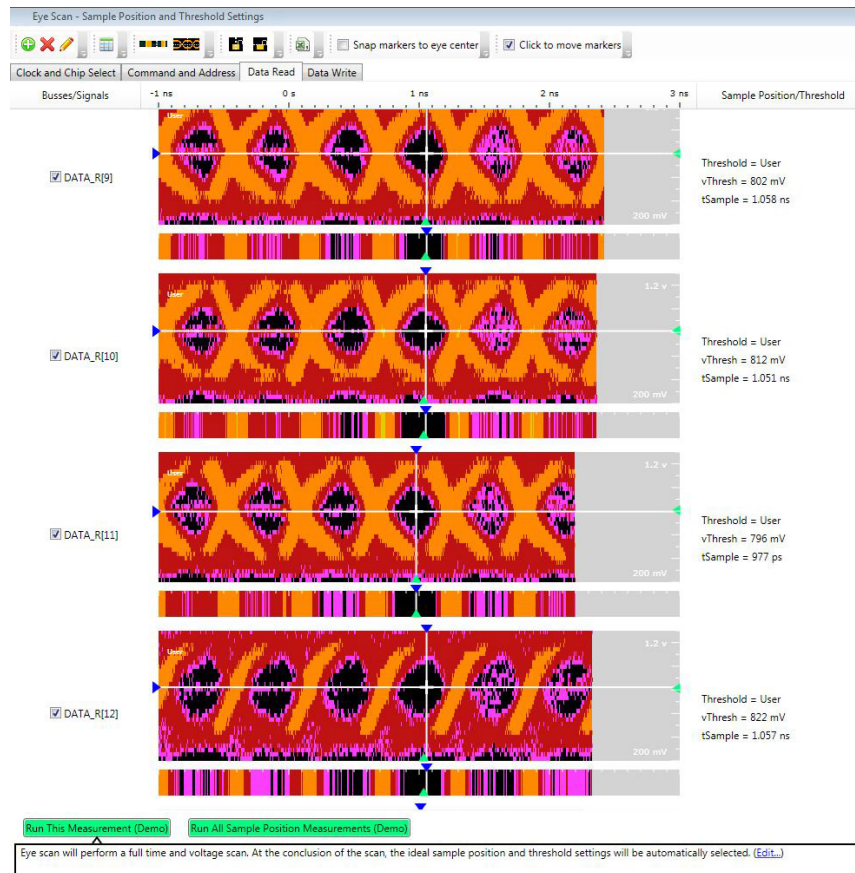# Protocol Analysis

The W3630A series BGA probes along with the B4621B memory bus decoder provide protocol decode of memory transactions using a Keysight logic analyzer as the analysis execution engine. Data is decoded and displayed at any level of detail from the protocol to binary. The B4621B protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed. The Keysight logic analyzer provides extensive triggering and store qualification features. The DDR protocol-decode software executes in the logic analyzer and takes user input on system attributes such as Burst length, CAS and Additive Latency, as well as Chip Selects to decode the key DDR bus signals and present a display that lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display. The W3630A Series BGA probes along with the B4622B DDR protocol compliance and analysis toolset provide physical address triggering, debug and compliance verification measurements.

Figure 4. Reliable protocol decode with B4621B DDR3 bus decoder

DDR3 BGA Probe Connection to an Oscilloscope

The DDR3 BGA probe is used with W3635B scope probe adapter and the E2678A socketed probe head to connect to the oscilloscope. The socketed probe head makes a 4 GHz bandwidth (typical) connection with the pin headers on the W3635B scope probe adapter with N5465A InfiniiSim Waveform Transformation toolset.
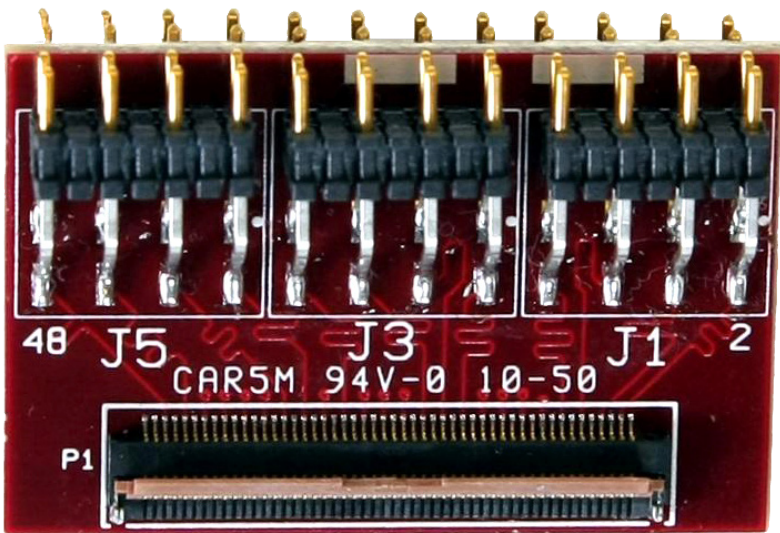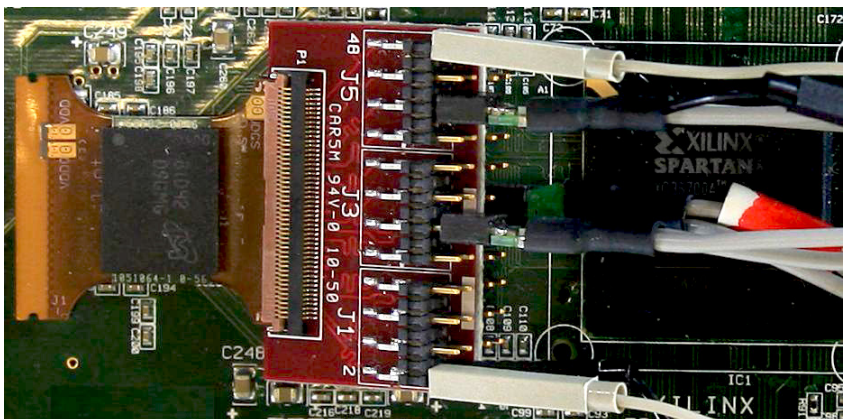

Figure 5. W3635B scope probe adapter

Figure 6. Probe connection to the oscilloscope with E2678A socketed probe head and probe connection to the MSO oscilloscope with E5383A single-ended flying lead set

Probe Pin-Out to Logic Analyzer and Scope

The following signals are omitted from the logic analyzer connection for the W3631A x16 probe system:

Address signal group
A15

Control signal group
BA2
CS2#, CS3#
VREFCA, VREFDQ
ZQ3, ZQ2, ZQ1, ZQ0

Data signal group
DMU
DQSL, DQSL#

Six signals are available for probing on the flex portion of the x16 rigid/flex solder-down probe:

CS2#, CS3#
VREFCA, VREFDQ
VDD, VDDQ

Table 1. W3631A x16 DDR3 BGA probe (for stacked DRAM <2G) pin out

	Left wing			Right wing	
Pin	Signal name	Group	Pin	Signal name	Group
All odd pins	GND	–	50	GND	–
2	DQU7	Data	48	DQU4	Data
4	DQU5	Data	46	DQU6	Data
6	DQU1	Data	44	DQSU#	Data
8	DQU3	Data	42	DQSU	Data
10	DQL0	Data	40	DQU2	Data
12	DQL2	Data	38	DQU0	Data
14	DQL6	Data	36	DML	Data
16	DQL4	Data	34	DQL1	Data
18	ODT1	Control	32	DQL3	Data
20	RAS#	Control	30	DQL7	Data
22	ODT0	Control	28	DQL5	Data
24	CAS#	Control	26	CK	Control
26	CS0#	Control	24	CK#	Control
28	CS1#	Control	22	CKE1	Control
30	WE#	Control	20	CKE0	Control
32	BA0	Control	18	A10/AP	Address
34	A3	Address	16	A12/BC#	Address
36	A0	Address	14	BA1	Control
38	A5	Address	12	A4	Address
40	A2	Address	10	A1	Address
42	A7	Address	8	A6	Address
44	A9	Address	6	A11	Address
46	RESET#	Control	4	A8	Address
48	A13	Address	2	A14	Address
50	GND	–	All odd pins	GND	–

The following signals are omitted from the logic analyzer connection for the W3636A x16 probe system:

Address signal group
None

Control signal group
CS1#, ODT1, CKE1
CS2#, CS3#
VREFCA, VREFDQ
ZQ3, ZQ2, ZQ1, ZQ0

Data signal group
DMU
DQSL#

Six signals are available for probing on the flex portion of the x16 rigid/flex solder-down probe:

CS2#, CS3#
VREFCA, VREFDQ
VDD, VDDQ

Table 2. W3636A x16 DDR3 non-stacked DRAM

	Left wing			Right wing	
Pin	Signal name	Group	Pin	Signal name	Group
All odd pins	GND	–	50	GND	–
2	DQU7	Data	48	DQU4	Data
4	DQU5	Data	46	DQU6	Data
6	DQU1	Data	44	DQSU#	Data
8	DQU3	Data	42	DQSU	Data
10	DQL0	Data	40	DQU2	Data
12	DQL2	Data	38	DQU0	Data
14	DQL6	Data	36	DML	Data
16	DQL4	Data	34	DQL1	Data
18	DQSL	Data	32	DQL3	Data
20	RAS#	Control	30	DQL7	Data
22	ODT0	Control	28	DQL5	Data
24	CAS#	Control	26	CK	Control
26	CS0#	Control	24	CK#	Control
28	WE#	Control	22	A10/AP	Control
30	BA2	Control	20	CKE0	Control
32	BA0	Control	18	A15	Address
34	A3	Address	16	A12/BC#	Address
36	A0	Address	14	BA1	Control
38	A5	Address	12	A4	Address
40	A2	Address	10	A1	Address
42	A7	Address	8	A6	Address
44	A9	Address	6	A11	Address
46	RESET#	Control	4	A8	Address
48	A13	Address	2	A14	Address
50	GND	–	All odd pins	GND	–

Probe Pin-Out to Logic Analyzer and Scope

The following signals are omitted from the Logic Analyzer connection for the x4/x8 probe system:

Address signal group
    None

Control signal group
    CS2#, CS3#
    VREFCA, VREFDQ
    ZQ3, ZQ2, ZQ1, ZQ0

Data signal group
    None

Table 3. W3633A x4/x8 DDR3 BGA probe pin out

Left wing			Right wing		
Wing pin	**Signal name**	**Group**	**Wing pin**	**Signal name**	**Group**
All odd pins	GND	–	50	GND	–
2	DQ0	Data	48	–	–
4	DQ2	Data	46	–	--
6	DQS	Data	44	–	–
8	DQS#	Data	42	–	–
10	DQ6	Data	40	–	–
12	DQ4	Data	38	DM	Data
14	–	–	36	DQ1	Data
16	RAS#	Control	34	DQ3	Data
18	ODT1	Control	32	DQ7	Data
20	CAS#	Control	30	DQ5	Data
22	ODT0	Control	28	CK	Control
24	WE#	Control	26	CK#	Control
26	CS0#	Control	24	CKE1	Control
28	CS1#	Control	22	CKE0	Control
30	BA2	Control	20	A10/AP	Address
32	BA0	Control	18	A15	Address
34	A0	Address	16	A12/BC#	Address
36	A3	Address	14	BA1	Control
38	A5	Address	12	A4	Address
40	A2	Address	10	A1	Address
42	A7	Address	8	A6	Address
44	A9	Address	6	A11	Address
46	RESET#	Control	4	A8	Address
48	A13	Address	2	A14	Address
50	GND	–	All odd pins	GND	–

Probe Pin-Out to Logic Analyzer and Scope (continued)

Table 4. W3631A with W3635B pin out

Left wing (W3631A)											
DQU7	DQU5	DQU1	DQU3	ODT1	RAS#	ODT0	WE#	A3	A0	RESET#	A13
DQL0	DQL2	DQL6	DQL4	CAS#	CS0#	CS1#	BA0	A5	A2	A7	A9

All ODD numbered pins are GND

A14	A8	A11	A6	A10	CKE0	CKE1	DQL7	DQL1	DML	DQU6	DQU4
A1	A4	BA1	A12	CK#	CK	DQL5	DQL3	DQU0	DQU2	DQSU	DQSU#
Right wing (W3631A)											

Table 5. W3636A with W3635B pin out

Left wing (W3636A)											
DQU7	DQU5	DQU1	DQU3	ODT1	RAS#	ODT0	BA2	A3	A0	RESET#	A13
DQL0	DQL2	DQL6	DQL4	CAS#	CS0#	WE#	BA0	A5	A2	A7	A9

All ODD numbered pins are GND

A14	A8	A11	A6	A10	CKE0	A10/AP	DQL7	DQL1	DML	DQU6	DQU4
A1	A4	BA1	A12	CK#	CK	DQL5	DQL3	DQU0	DQU2	DQSU	DQSU#
Right wing (W3636A)											

Probe Pin-Out to Logic Analyzer and Scope (continued)

Table 6. W3633A with W3635B pin out

Left wing (W3633A)											
DQ0	DQ2	DQS	DQS#	ODT1	CAS#	ODT0	BA2	A0	A3	RESET#	A13
DQ6	DQ4	NC	RAS#	WE#	CS0#	CS1#	BA0	A5	A2	A7	A9

All ODD numbered pins are GND											

A14	A8	A11	A6	A15	A10	CKE0	DQ5	DQ3	DQ1	NC	NC
A1	A4	BA1	A12	CKE1	CK#	CK	DQ7	DM	NC	NC	NC
Right wing (W3633A)											

Logic Analyzer Configuration Guide and Ordering Information

DRAM type	Data width	Access to	Probes	Cables	Logic analyzer modules	Order summary
DDR3 78 ball x4/x8	x4/x8*	Command, Address, Control and Data	W3633A	E5847A	16962A x 2	16962A 2 E5847A 1 W3633A 1
				E5847A U4201A (4)	U4154A	U4154A U4201A 4 E5487A 1 W3633A 1
DDR3 96 ball x16 stacked DRAM under 2G deep	x16	Command, Address, Control and Data	W3631A	E5845A	16962A 2	16962A 2 E5845A 1 W3631A 1
				E5845A U4201A (4)	U4154A	U4154 U4201A 4 E5845A 1 W3631A 1
DDR3 96 ball x16 un-stacked DRAM	x16	Command, Address, Control and Data	W3636A	E5845A	16962A 2	16962A 2 E5845A 1 W3636A 1
				E5845A U4201A (4)	U4154A	U4154 U4201A 4 E5845A 1 W3636A 1

U4154A requires M9502A or M9505A AXIe chassis.
16962A requires 16900 series chassis.

*Each DRAM probe requires one W3633A BGA interposer and one E5847A cable.

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Logic Analyzer Configuration Guide and Ordering Information

Product	Description
DDR3 BGA probes	
W3631A	DDR3 x16 BGA command and data probe for logic analyzer and oscilloscope
W3636A	DDR3 x16 non-stacked DRAM BGA command and data probe for logic analyzer and oscilloscope
W3633A	DDR3 x4/x8 BGA command and data probe for logic analyzer and oscilloscope
AXIe modular logic analyzers	
U4154A	136-channel, 4 Gb/s state, 5 GHz timing, memory depth up to 200 M, AXIe-based logic analyzer module
U4201A (4)	Logic analyzer probe cable
AXIe based modular chassis	
M9502A	Two slot chassis
M9505A	Five slot chassis
M9536A	Embedded controller for use with AXIe based chassis
16900 Series logic analyzers	
16902B	6-slot mainframe with 15-inch display with touch screen
16900 Series logic analyzer modules [1]	
16962A	68-ch, 2 GHz timing, 2 GT/s State, 4 M deep logic analysis module
Logic analyzer ZIF probes [2]	
E5845A	46-ch single-ended ZIF probe for x16 DRAM BGA probe connect to 90-pin logic analyzer cable
E5847A	46-ch single-ended ZIF probe for x8 DRAM BGA probe connect to 90-pin logic analyzer cable
Software	
B4621B	DDR bus decoder
B4622B	DDR protocol compliance and analysis tool set
DDR Setup Assistant and DDR Eyefinder [3]	Recommended

1. 16962A uses a separate DDR3 EyeFinder/EyeScan SW tool. U4154A EyeFinder/ EyeScan SW is part of U4154A SW package.
2. Used to connect W3630As Series DDR3 BGA probes to 90 pin logic analyzer cables.
3. DDR Setup Assistant and Eyefinder software is available free of charge. DDR Setup Assistant provides a series of steps to simplify state mode measurement tuning with U4154A or 16962A logic analyzer modules. The DDR Setup Assistant and Eyefinder software also provides a DDR Eyefinder tool specifically for the 16962A module.

Oscilloscope Ordering Information

Product	Description
W3635B	Scope board probe adapter for use with W3630A Series DDR3 BGA probe – Kit of 2
Oscilloscope	
90604A	6 GHz 4 channels 20 GSa/s Infiniium oscilloscope
90804A	8 GHz 4 channels 40 GSa/s Infiniium oscilloscope
91204A	12 GHz 4 channels 40 GSa/s Infiniium oscilloscope
91304A	13 GHz 4 channels 40GSa/s Infiniium oscilloscope
X91604A	16 GHz 4 channel 80 GSa/s Infiniium oscilloscope
X92004A	20 GHz 4 channel 80 GSa/s Infiniium oscilloscope
X92504A	25 GHz 4 channel 80 GSa/s Infiniium oscilloscope
X92804A	28 GHz 4 channel 80 GSa/s Infiniium oscilloscope
X93204A	32 GHz 4 channel 80 GSa/s Infiniium oscilloscope
Oscilloscope software packages	
U7231A	DDR3 Compliance Test Application
N5414B	InfiniiScan Event Identification Software
N5465A	InfiniiSim Waveform Transformation Toolset
Oscilloscope probe amplifier	
1169A	12 GHz InfiniiMax differential probe amplifier
1168A	10 GHz InfiniiMax differential probe amplifier
1134A	7 GHz InfiniiMax differential probe amplifier
Oscilloscope probe heads	
E2678A	InfiniiMax single-ended/differential socketed probe head and accessories

Related Literature

Publication title	Pub number
U4154A AXIe-based Logic Analyzer Module – Data Sheet	5990-7513EN
Keysight W3630A Series DDR3 DRAM BGA Probe	5990-3179EN
B4622B DDR2/3/4 and LPDDR/2/3 Protocol Compliance and Analysis Toolset – Data Sheet	5991-1063EN
U7231A DDR3 Compliance Test Application for Infiniium Series Oscilloscopes – Data Sheet	5989-7243EN
A Time-Saving Method for Analyzing Signal Integrity in DDR Memory Buses – Application Note	5989-6664EN
Infiniium 90000-X Series Oscilloscopes – Data Sheet	5990-5271EN
B4621B for DDR2, DDR3, or DDR4 Debug and Validation – Data Sheet	5991-0802EN
Advanced Probe Settings Mode – Technical Overview	5991-0799EN
Keysight Technologies 16900 Series Logic Analysis Systems – Brochure	5989-0420EN

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